Programmes After Market Services NHP-2 Series Transceivers

# 9. Troubleshooting

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# Transceiver Troubleshooting

# **Baseband Description**

The baseband module is a CDMA dual-band engine. Baseband architecture is based on the DCT4 Apollo engine. The baseband consists of three new ASICs: Universal Energy Management (UEM), Universal Phone Processor (UPP), and Flash 64 Megabit.

The baseband architecture supports a power-saving function called "sleep mode". This sleep mode shuts off the VCTCXO, which is used as a system clock source for both RF and Baseband. During the sleep mode, the system runs from a 32 kHz crystal. The phone is wakened by a timer running from this 32 kHz clock supply. The sleep time is determined by network parameters. Sleep mode is entered when both the MCU and the DSP are in standby mode and the normal VCTCXO clock is switched off.

NHP-2 supports both three- and two-wire types of DCT3 chargers. There is a separate PWM output for controlling the three-wire charger. Charging is controlled by the UEM ASIC and by EM SW running in the UPP.

# **BB** and **RF** Architecture





# Power Up and Reset

Power up and reset is controlled by the UEM ASIC. There are three ways to power up the baseband module:

1 Power Button (grounding the PWRONX pin of the UEM).

- 2 Connect the charger to the charger input.
- 3 RTC Alarm (when the RTC logic has been programmed to give an alarm).



Figure 2: UEM start-up sequence from reset to power-on mode



#### Troubleshooting

First, carry out a thorough visual check of the module. Make sure that:

- there are no mechanical damages
- solder joints are OK

Before changing anything, ALL SUPPLY VOLTAGES AND SYSTEM CLOCK / SLEEP CLOCK should be checked.

#### Power up faults

*Power-up sequence* 

UEM acts as a HW master during start up

- 1 VBATT limits: 2.1V for internal state machine, 3V triggering whole startup
- 2 Regulator sequencing
  - Hw "core" regulators "on": VANA, VIO, VFLASH1, VFLASH2, and VCORE, which provide nominal voltages and currents according to Table 1.

Regulator	Maximum current (mA)	Vout (V)	Notes
VCORE (dc/dc)	300	1.5	Output voltage selectable 1.0V/1.3V/1.5V/1.8V. Power-up default: 1.5V
VIO	150	1.8	Always enabled, except during power-off mode.
VFLASH1	70	2.78	Always enabled, except during power-off mode.
VFLASH2	40	2.78	Enabled only when data cable is connected.
VANA	80	2.78	Enabled only when the system is awake. (Off during sleep mode and power-off mode.)

#### Table 1: Baseband regulators

• UEM supplies voltages VR1A, VR1B, VR2, VR3, VR4, VR5, VR6, and VR7 for RF. See Table 2.

Regulator	Maximum current (mA)	Vout (V)	Notes
VR1A	10	4.75	Enabled when receiver is on.
VR1B	10	4.75	Enabled when transmitter is on
VR2	100	2.78	Enabled when transmitter is on
VR3	20	2.78	Enabled when SleepX is high
VR4	50	2.78	Enabled when receiver is on
VR5	50	2.78	Enabled when receiver is on
VR6	50	2.78	Enabled when transmitter is on
VR7	45	2.78	Enabled when receiver is on

#### Table 2: RF regulators

- 3 Reset releasing delay
  - Supply voltages stabilize to their UEM hw default value
  - RFCLK grows to full swing
  - Core is ready to run but waiting for PURX release
- 4 Reset releasing
  - UPP releases the SLEEPX up to "non sleep" -state to prevent the UEM switching the regulators "OFF"

- 5 MCU starts running the Bootsrap Code
  - written in stone/ UPP internal ROM
  - the program checks if there exists any reason for FDL mode (Flash Down Load)
  - If there exists executable code in FLASH and there exists no reason for FDL, the MCU starts running the MCU program from FLASH.
- 6 MCU runs the FLASH MCU code the phone initialization, user interfaces, internal blocks, etc.
  - Core regulator voltage setting for required DSP speed
  - Initializes the DSP and concerning hw

#### Releases DSP reset -> DSP starts running

- 1 Power key pressed
  - After 20ms, UEM enters RESET MODE if VBAT>Vmstr+
  - VFLASH1, Vana, Vcore, Vio, and VR3 goes high.
  - VCTCXO enabled by VR3 -> RFClk 19.44 MHz running.
- 2 Purx released
  - Purx released by UEM, UEMINT goes high for 100 ms, SleepX goes high and SleepClk (32 KHz) starts running.
- 3 Software running
  - Default value of Vcore is 1.5 V.
  - Cbus (1.2MHz) and Dbus (9.6MHz) clocks start running.

Note! In case of power up faults, it's not possible to force phone on by disabling watchdog. Instead it's recommended to use normal or single triggering on oscilloscope, so that it's possible to see if signal goes to its normal value even for a while when power key is pressed.

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## Phone is totally dead



# Phone Doesn't Stay On or Phone is Jammed





# Flash programming

# Connections to Baseband

The flash programming equipment is connected to the baseband using test pads for galvanic connection. Test pads are allocated in such a way that they can be accessed when the phone is assembled. The flash programming interface uses the VPP, FBUSTX, FBUSRX, MBUS, and BSI connections for connection to the baseband. The connection is through the UEM, which means that the logic levels correspond to 2.7V. Power is supplied using the battery contacts.

Baseband power is controlled by the flash prommer in production and in reprogramming situations. When supply voltage is applied to the battery terminals, the baseband will power up.

#### Flash programming procedure

• Phone communicates with prommer via production test pattern, using signals:

FBUSTX (serial data to phone),

FBUSRX (Serial data from phone),

MBUS (serial clock for FBUSRX)

VPP (External flashing voltage for speed up flashing)

Also BSI line is used when initializing flashing(battery connector)

- When phone has entered flash programming mode, prommer indicates to UEM that flash programming will take place by writing 8-bit password to UEM. Prommer will first set BSI to "1" and then uses FBUSRX for writing and MBUS for clocking. After that, BSI is reset to "0".
- MCU indicates to prommer that it has been noticed, by using the FBUSTX signal. After this, it reports UPP type ID and is ready to receive secondary boot code to its internal SRAM.



#### Figure 3: Flashing start

 This boot code asks MCU to report prommer phone's configuration information, including flash device type. Now, the prommer can select and send algorithm code to MCU SRAM (and SRAM/Flash self-tests can be executed).







Figure 5: Flashing, continued

Flash programming error codes

- Error codes can be seen from the test results or from Phoenix's flashtool\*
- Underlined note means that the connection under consideration is being used for the first time.
- Some error codes may be added later. Here are the most common ones.

Error	Description	Not working properly
C101	"The Phone does not set FbusTx line high after the startup."	Vflash1 VBatt BSI and FbusRX from prommer to UEM. FbusTx from UPP->UEM->Prommer(SA0)
C102	"The Phone does not set FbusTx line low after the line has been high. The Prommer generates this error also when the Phone is not connected to the Prommer."	PURX(also to Safari)   VR3   Rfclock(VCTCXO->Safari->UPP)   Mbus from Prommer->UEM-   >UPP(MbusRx)(SA0)   FbusTx from UPP->UEM->Prommer(SA1)   BSI and FbusRX from prommer to UEM.
C103	" Boot serial line fail."	Mbus from Prommer->UEM- >UPP(MbusRx) <u>(SA1)</u> FbusRx from Prommer-> <u>UEM-&gt;UPP</u> FbusTx from UPP->UEM->Prommer
C104	"MCU ID message sending failed in the Phone."	FbusTx from UPP->UEM->Prommer

Table 3: Flash programming error codes

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C105	"The Phone has not received Secondary boot codes length bytes correctly."	Mbus from Prommer->UEM- >UPP(MbusRx) FbusRx from Prommer->UEM->UPP FbusTx from UPP->UEM->Prommer
C106	"The Phone has not received Secondary code bytes correctly."	Mbus from Prommer->UEM- >UPP(MbusRx) FbusRx from Prommer->UEM->UPP FbusTx from UPP->UEM->Prommer
C107	"The Phone MCU can not start Secondary code correctly."	UPP
C586	"The erasing status response from the Phone informs about fail."	Flash
C686	"The programming status response from the Phone informs about fail."	Flash
Cx81	"The Prommer has detected a checksum error in the message, which it has received from the Phone."	FbusTx from UPP->UEM->Prommer
Cx82	"The Prommer has detected a wrong ID byte in the message, which it has received from the Phone."	FbusTx from UPP->UEM->Prommer
A204	" The flash manufacturer and device lds in the existing Algo- rithm files do not match with the lds received from the target phone."	<u>Flash</u> UPP VIO/VANA? Signals between UPP-Flash
Cx83	"The Prommer has not received Phone acknowledge to the message."	Mbus from Prommer->UEM- >UPP(MbusRx) FbusRx from Prommer->UFM->UPP
Cx84	"The Phone has generated NAK signal during data block trans-	FbusTx from UPP->UEM->Prommer
Cx85	fer."	
	"Data block handling timeout"	
Cx87	"Wrong MCU ID."	RFClock UPP(Vcore)
Startup for flashing	Required startup for flashing	Vflash1 VBatt

Flash programming





# **Charging Operation**

A Lithium-ion battery with a capacity of 920 mAh is used in NHP-2. Temperature and capacity information are needed for charge control. These resistors are connected to the BSI and BTEMP pins of battery connector. The phone has 100 kW pull-up resistors for these lines so that they can be read by A/D inputs in the phone.



Figure 6: BLB-3 battery pack pin order

Charging circuitry

The UEM ASIC controls charging, depending on the charger being used and the battery size. External components are needed for EMC, reverse polarity, and transient protection of the input to the baseband module. The charger connection is through the system connector interface. NHP-2 baseband is designed to support DCT3 chargers from an electrical point of view. Both two- and three-wire chargers are supported.





# Charger Detection

Connecting a charger creates voltage on VCHAR input of the UEM. When VCHAR input voltage level is detected to rise above 2 V (VCHdet+threshold) by UEM, charging starts. VCHARDET signal is generated to indicate the presence of the charger for the SW. The charger identification/acceptance is controlled by EM SW.

The charger recognition is initiated when the EM SW receives a "charger connected" interrupt. The algorithm basically consists of the following three steps:

1 Check that the charger output (voltage and current) is within safety limits.

- 2 Identify the charger as a two-wire or three-wire charger.
- 3 Check that the charger is within the charger window (voltage and current).

If the charger is accepted and identified, the appropriate charging algorithm is initiated.



Figure 8: Charging circuit

# Charger troubleshooting



#### Display and Keyboard

LEDs are used for LCK and keypad illumination in NHP-2. There are six LEDs for the LCD and six LEDs for the keypad.

A black/white LCD is used in NHP-2. Interface uses 9-bit data transfer. The interface is similar to DCT3-type interface, except that Command/Data information is transferred together with the data. D/C bit set during each transmitted byte.



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# **Keypad faults**







#### Audio

Audio control and processing in NHP-2 is accomplished by UEM, which contains the audio codec, and by UPP, which contains the MCU and DSP blocks, handling and processing the audio data signals.

The baseband supports three microphone inputs and two earpiece outputs. Microphone

inputs are MIC1, MIC2, and MIC3. MIC1 input is used for the phone's internal microphone; MIC2 input is used for headsets or loopset. MIC3 input is used for third-party accessories (2.5mm Jack).

Every microphone input can have either a differential or single-ended AC connection to UEM circuit. In NHP-2, the internal microphone (MIC1) is differential, whereas MIC2 and MIC3 microphones for accessory detection are single-ended. The microphone signals from different sources are connected to separate inputs at UEM. Inputs for the microphone signals are differential type. Also, MICBIAS1 is used for MIC1 and MIC3 and MICBIAS2 is used for MIC2.

#### Accessories

NHP-2 supports single-ended external audio accessory connection. Headset and data cables can be connected directly to the system connector or 2.5mm jack supporting TTY/ TDD or third-party accessories. Detection of different accessories is made in analog mode by reading the DC voltage value of its corresponding AD converter. The following table indicates accessory detection levels.

Columbia Accessory Detection Table Limits									
Accessory	ADC Low	er Limit	ADC Upper Limit		ADC used		Interrupt	Interrupt to	
Туре	Voltage	Hex	Voltage	Hex	HEADINT	KEYB1	Detection	answer/end call	
	Value	Value	Value	Value					
HDC_9P	0.50V	0×012	400mV	0x094	×	N/A	HEADINT	HOOKIN T	
HDE-1	0.50V	0×012	400mV	0×094	×	N/A	HEADINT	N/A	
LPS-1	0.50V	0x012	400mV	0×094	×	N/A	HEADINT	N/A	
DLR-3P	500mV	0×0B9	850mV	0x13A	×	N/A	HEADINT	N/A	
JBA-4	900mV	0×14B	1400mV	0x202	×	N/A	HEADINT	N/A	
Third Party Acc.	0.50V	0×012	1.0V	0×170	N/A	×	GenIO21	N/A	
TTY/TDD	2.40V	0x374	2.78V	0x3FF	N/A	×	GenIO21	N/A	

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# Audio Troubleshooting







Buzzer failure



# Receiver fault finding



Figure 9: Receiver block diagram

#### General instructions for RX troubleshooting

Start Phoenix software and use it to start the wanted RX-mode of the mobile phone. Troubleshooting flowchart is divided into three steps: general checking, local checking, and RX-chain checking. Notice that before changing ASICs or filter, all solderings and missing components must be checked visually. After any possible component changes, the phone must be retuned.

#### Path of the received signal

Block level description of the receiver:

(Antenna/ext RF) Antenna Switch – Diplexer – Duplexer – Low Noise Amplifier (LNA) – RX band filter – First mixer – 128.1 MHz RX IF filter – IF-amplifier – second mixer – 614 kHz low-pass filter – adjustable IQ amplifier – Baseband.

# AMPS Using Phoenix, configure phone AGC & audio routing to make SINAD measurement Apply 881.49 MHz = ch 383 -116dBm, 8kHz dev, 1kHz sine signal to external RF-connector X800. YES ▼ Connect HS to cellular tester; open audio AF: 1kHz sine signal, NO-AMPS RX-chain OK meas SINAD AF:>12 dB YES ▼ Check UHF Vc (from Start synthesizer NO-C509) V: 1.8...2.1V troubleshooting YĖS ▼ Check RXVHF Vc Start synthesizer (from C715), NOtroubleshooting V:0.7...1.3 Using Phoenix, readjust AGC to obtain proper Rx I/Q level Apply 881.49 MHz -30dBm, sine signal to external RF-connector X900.

#### Fault finding charts for receiver chain





# Cell CDMA

## Troubleshooting 128.1 MHz IF Saw Filter

Since the same physical signal path is used for both analog and digital modes at the lower band, there is no need for additional troubleshooting in the digital mode. So if the digital mode at the lower band is not working properly, start the analog mode trouble-shooting.

#### PCS

Only EXT RF connector  $\rightarrow 1^{st}$  IF needs separate troubleshoot at upper band. After down conversion (RF  $\rightarrow 128.1$  MHz) both lower and upper band use same signal path.







# Transmitter fault finding



Figure 10: Transmitter block diagram

# General instructions for TX troubleshooting

Always use RF-cable connected from external RF-connector to analyzer via (rf-power) attenuator. This is important to protect analyzer against excessive rf-power and to prevent unwanted rf-power from leaking to the cellular frequencies.

Start Phoenix software and select TX mode. It is recommended that you select mid channel (383 for AMPS/CDMA or 600 for PCS) and appropriate power level.

Note: Tune the phone after any component change.

# Path of the transmitted signal

AMPS/Cell CDMA

UEM TX I/Q DA-converters -> I/Q modulator and VGA (Robin) -> IF -> Upconverter + driver - EXT Driver amp > BPF -> PA -> (Power detector) -> Duplex-filter -> Diplexer -> EXT RF-connector -> Cyclops -> Antenna

# PCS (ONLY DUALBANDER)

UEM TX I/Q DA-converters -> I/Q modulator and VGA (Robin) -> IF-> Upconverter + driver ->Balun -> BPF -> PA-> (Power detector) -> Duplex-filter -> Diplexer -> EXT RF-connector -> Cyclops -> Antenna

Power detection and power control circuit belongs under power control part of this guide.

# Fault finding charts for transmitter

#### AMPS

Start Phoenix software and set phone to the Analog mode. Set channel 383 and Powerlevel 2. Connect RF-cable to Ext RF connector and connect cable to Spectrum analyzer input and measure RF level. Please notice insertion loss of the cable and attenuations.





# Cell CDMA

The transmitter chain is exactly same as AMPS mode, except control current. Thus, it is important that AMPS has no faults.

# PCS (only dualbander)

PCS mode and Cell CDMA mode have a common RF modulator, making it important that Cell CDMA mode has no faults.





# Power control loop

Basically power detection is done with circuitry and power control is done inside Robin and PA. Power detection is basically similar for both bands, except both bands have individual couplers.



Detected voltages are described in the next table and diagram.

TYPICAL DETECTED VOLTAGES AT POWER LEVELS PL2PL10 FOR DUALBANDER														
800A					800D					1900D				
	Pout	TXPWRDET		TXPWRDET			Pout	TXPWRDET			Pout	TXPWRDET		
PL	dBm	dac	mV		dBm	dac	mV		dBm	dac	mV			
2	26.5	633	1671		27.3	696	1839		27.3	662	1746			
3	22.5	393	1038		23.3	433	1142		23.3	405	1069			
4	18.5	237	625		19.3	261	688		19.3	245	648			
5	14.5	141	372		15.3	155	410		15.3	147	387			
6	10.5	82	215		11.3	90	237		11.3	84	222			
7	6.5	46	120		7.3	50	132		7.3	46	122			
8	-	-	-		3.3	27	70		3.3	24	64			
9	-	-	-		-0.7	13	33		-0.7	11	30			
10	-	-	-		-4.7	5	12		-4.7	5	12			

NOTE: DAC VALUES MAY VARY ABOUT +/- 20%



# Synthesizer fault finding

There are four oscillators generating the needed frequencies for RF-section. 19.2 MHz reference oscillator, 1 GHz and 2GHz UHF VCO, TX VHF VCO, and RX VHF VCO. RX VHF frequency is fixed 256.2 MHz and TX VHF has two fixed frequencies: 246.2 MHz for low-band and 416.2 MHz for upper band. UHF VCO's operating frequencies are controlled by PLL-circuit of LMX2370I. All locals are locked to stable 19.2 MHz reference oscillator.

The frequency range for UHF VCO is two separate bands. The output frequency range for the lower band is from 997.11 MHz to 1022.07 MHz. In upper band, the output frequency range from the UHF VCO is from 2058.1 MHz to 2118.05 MHz.

It is practical to check out the synthesizer status by measuring control voltage of the VCO from the Integrator capacitor. If the voltage is stable and reasonable, local oscillators are running correctly.

#### 19.2 MHz reference oscillator

The 19.2 MHz oscillator frequency (G790) is controlled by UEM. This 19.2 MHz signal is connected to Batman/Robin and there in PLL-circuits and to UPP.

All synthesizers use divided VCTCXO signal as a reference signal for Phase locked loop to provide correct LO-frequency.

Baseband needs a reference signal where it can generate the necessary clock signals and VCTCXO output signal is also buffered and connected to UPP.

## Fault finding chart for 19.2 MHz oscillator



## **RX VHF VCO**

The RX VHF VCO signal is used to generate receiver Intermediate frequency. RX VHF VCO has one fixed frequency 256.2 MHz. Operating frequency is locked in Phase-locked Loop.

RX VHF VCO output signal is fed to Batman. Inside, the Batman signal is divided for Phase detector and RX parts. Before I/Q-modulator frequency is divided by 2.

#### Fault finding chart for RX VHF VCO

Measure oscillator frequency over L701 coil. Don't connect probe to pads!



#### **TX VHF Synth**

The TX VHF VCO signal is used to generate transmitter Intermediate frequency. TX VHF VCO has two fixed frequencies: 346.2 MHz for lower band and 416.2 MHz for upper band. Operating frequency is locked in Phase-locked Loop and frequency is divided by two before modulator.

## Fault finding chart for TX VHF VCO

AMPS, CH383 -> TX VHF frequency 346.2 MHz



#### **UHF Synthesizer**

The UHF synthesizer consists of an external UHF VCO, loop filter and integrated PLL in LMX2370 N501. IC contains stages like counters, prescaler, divider by two, phase and frequency comparator, and a charge pump circuit.

The output frequency of the VCO depends on the DC-control voltage, which is controlled by PLL-circuit inside N501.

# Fault finding chart for UHF Synthesizer



# **Test Point Diagrams**





Figure 11: Test points — top view A



Figure 12: Test points — top view B



Figure 13: Test points — bottom view A



Figure 14: Test points — bottom view B